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06EC74

Seventh Semester B.E. Degree Examination, June/July 2013
DSP Algorithms and Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. List and explain the issues that have to considered in designing and implementing a DSP system. **(04 Marks)**

b. Implement an FIR filter for $y(n) = \frac{(x(n) + x(n-1) + x(n-2))}{3}$. Determine the (i) system function (ii) magnitude response function (iii) phase response function. Plot its magnitude and phase response. **(06 Marks)**

c. Explain the process of decimation. **(04 Marks)**

d. The signal sequence x(n) = [0 2 4 6 8] is interpolated using the interpolation filter sequence b_k = [0.5 1 0.5] and the interpolation factor is 2. Determine the interpolated sequence y(m). **(06 Marks)**

2 a. Explain the different frequently used techniques to prevent overflow and underflow conditions occurring in MAC unit. **(04 Marks)**

b. Explain the different ways in which the on-chip memory can be organized efficiently and cost-effective manner. **(04 Marks)**

c. Explain the register pointer updating algorithm for circular buffer addressing mode. **(04 Marks)**

d. List the techniques used in DSP architecture to increase speed of operation and operations that should be accomplished in single clock to achieve parallelism in DSP iomplementation. **(08 Marks)**

3 a. Explain with a neat clock diagram the indirect addressing mode of TMS320C54XX processor. Give the operand syntax and operation for the following:
i) Circular addressing mode ii) Bit reverse addressing mode. **(10 Marks)**

b. Explain the different ways in which PC addresses the program memory either on-chip or off-chip and gets loaded for execution of instructions. **(06 Marks)**

c. Specify the on-chip memory configuration for MP/$\overline{MC}$, OVLY and DROM located in processor mode status register of 5416 processor. **(04 Marks)**

4 a. Describe the operation and application of the following instructions of TMS320C54XX processor with example:
i) MAC ii) MAS iii) LD *AR4, 4, A
Given contents of AR4 is 8boeh& S×M = 1. Determine the contents of accumulator. **(06 Marks)**

b. Write an ALP of TMS320C54XX processor to compute
y(n) = h cos x(n) + h(1) x(n – 1) + h(2) x(n – 2) , using MAC instruction, where h(0) = 5, h(1) = 31, h(2) = 13 are in program memory locations starting at h. x(n) = 1, x(n – 1) = 5 x(n – 2) = – 3 are in data memory locations starting at x.y(n) is to be saved (lower 16 bits) in location y and y +1 (higher 16 bits). **(05 Marks)**

c. With a neat sketch, describe the Host port interface signals. **(04 Marks)**

d. Explain the six-stage pipelined execution of TMS320C54XX. **(05 Marks)**

PART – B

5 a. Define Q Notation. Explain Q_7 and Q_{15} Notations with example. **(05 Marks)**

b. Realize and write a program for a second order IIR filter on TMS320C54XX processor defined by the transfer function $H(z) = \frac{0.104 - 0.102z^{-1} + 0.104z^{-2}}{1 + z^{-1} - 0.612z^{-2}}$. Assume that the filter coefficients are q_{15} numbers x(n) is the input sample (integer), input samples are placed in buffer, insamples, from a data file, data_in.dat. y(n) is computed output. The output samples are placed in a buffer outsamples. **(10 Marks)**

c. Explain with necessary block diagram, memory organization for implementing FIR filter of order N. **(05 Marks)**

6 a. Determine the following for a 512 point FFT computation :
i) Number of stages ii) Number of butterflies in each stage iii) Number of butterflies needed for the entire computation. iv) Number of butterflies that need no twiddle factors. v) Number of butterflies that require real twiddle factors vi) Number of butterflies that require complex twiddle factors. **(06 Marks)**

b. Explain how scaling prevents overflow conditions in the butterfly computation. **(06 Marks)**

c. Write a TMS320C54XX program segment that implements 8 point DIT FFT bit reversed index generation and to clear FFT data memory. **(08 Marks)**

7 a. Interface an 8k×16 program ROM to the C5416 DSP in the address range 7FE000h – 7FFFFFh. **(06 Marks)**

b. Explain with a flow chart diagram for software polling for the programmed I/O A/D converter interface. **(06 Marks)**

c. Define interrupt. Write a flow chart of interrupt handling by C54XX processor. **(08 Marks)**

8 a. Explain with neat block diagram the PCM 3002 interfaced to TMS320VC5416 in the DSK. **(06 Marks)**

b. Explain with block diagram the biotelemetry receiver implementation. **(06 Marks)**

c. With a neat sketch, explain the JPEG encoder and decoder. **(08 Marks)**

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